In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently amended) An electronic fuse, comprising:

a latch; and

a nonvolatile memory element coupled to said latch, said nonvolatile memory element comprising a pair of floating gate devices sharing a common floating gate and configured to be programmed to a memory value capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

2. (Original) The electronic fuse of Claim 1, wherein said latch comprises cross-coupled inverters.

3. (Original) The electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

4. (Original) The electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

5. (Original) The electronic fuse of Claim 3, wherein said floating-gate transistor is a MOS device.

6. (Canceled)

7. (Original) The electronic fuse of Claim 3, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

8. (Original) The electronic fuse of Claim 3, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

9. (Original) The electronic fuse of Claim 3, wherein the amount of charge on the floating gate may be changed using direct tunneling.

10. (Original) The electronic fuse of Claim 3, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

11. (Canceled)

12. (Original) The electronic fuse of Claim 3, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with said floating gate of said floating-gate transistor.

13. (Original) The electronic fuse of Claim 12, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

14. (Original) The electronic fuse of Claim 1, further comprising a capacitive element coupled to an output of the latch.

15. (Original) The electronic fuse of claim 3, wherein the latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating-gate voltage is relatively low.

16. (Original) The electronic fuse of claim 15, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

17. (Original) The electronic fuse of claim 15, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

18. (Original) The electronic fuse of claim 15, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

19. (Currently amended) An electronic fuse, comprising:

a latch having two cross-coupled inverters; and

a nonvolatile memory element coupled between a power source terminal of the fuse and a first of the two inverters of said latch, said nonvolatile memory element comprising a pair of floating gate devices sharing a common floating gate and configured to be programmed to a memory value capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

20. (Canceled)

21. (Currently amended) The electronic fuse of Claim ~~20~~19, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

22. (Original) The electronic fuse of Claim 19, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

23. (Original) The electronic fuse of Claim 21, wherein said floating-gate transistor is a MOS device.

24. (Canceled)

25. (Original) The electronic fuse of Claim 21, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

26. (Original) The electronic fuse of Claim 21, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

27. (Original) The electronic fuse of Claim 21, wherein the amount of charge on the floating gate may be changed using direct tunneling.

28. (Original) The electronic fuse of Claim 21, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

29. (Canceled)

30. (Original) The electronic fuse of Claim 21, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with said floating gate of said floating-gate transistor.

31. (Original) The electronic fuse of Claim 30, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

32. (Original) The electronic fuse of Claim 19, further comprising a capacitive element coupled to an output of the latch.

33. (Original) The electronic fuse of claim 21, wherein the latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.

34. (Original) The electronic fuse of claim 33, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

35. (Original) The electronic fuse of claim 33, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

36. (Original) The electronic fuse of claim 33, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

37. (Currently amended) An electronic fuse, comprising:

a latch having two cross-coupled inverters; and

a nonvolatile memory element coupled in parallel with a transistor of a first of the two inverters of the latch, said nonvolatile memory element comprising a pair of floating gate devices sharing a common floating gate and configured to be programmed to a memory value capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

38. (Canceled)

39. (Currently amended) The electronic fuse of Claim ~~38~~37, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

40. (Original) The electronic fuse of Claim 38, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

41. (Original) The electronic fuse of Claim 39, wherein said floating-gate transistor is a MOS device.

42. (Canceled)

43. (Original) The electronic fuse of Claim 39, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

44. (Original) The electronic fuse of Claim 39, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

45. (Original) The electronic fuse of Claim 39, wherein the amount of charge on the floating gate may be changed using direct tunneling.

46. (Original) The electronic fuse of Claim 39, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

47. (Canceled)

48. (Original) The electronic fuse of Claim 39, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with said floating gate of said floating-gate transistor.

49. (Original) The electronic fuse of Claim 48, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

50. (Original) The electronic fuse of Claim 37, further comprising a capacitive element coupled to an output of the latch.

51. (Original) The electronic fuse of claim 39, wherein the latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.

52. (Original) The electronic fuse of claim 51, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

53. (Original) The electronic fuse of claim 51, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

54. (Original) The electronic fuse of claim 51, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross coupled inverters.

55. (Original) An electronic fuse, comprising:

a latch;

a first nonvolatile memory element coupled to a first node of the latch, said first nonvolatile memory element configured to be programmed to a first memory value; and

a second nonvolatile memory element coupled to a second node of the latch, said second nonvolatile memory element configured to be programmed to a second memory value,

wherein the first and second programmed memory values cause said latch to settle to a predetermined one of a first and a second state as a power-up or a reset signal is applied to the fuse, and wherein said first and second nonvolatile memory elements each comprises a pair of floating gate devices sharing a common floating gate, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

56. (Original) The electronic fuse of Claim 55, wherein said latch comprises cross-coupled inverters.

57. (Original) The electronic fuse of Claim 55, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value.

58. (Original) The electronic fuse of Claim 57, wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value.

59. (Original) The electronic fuse of Claim 57, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with said first floating gate of said first floating-gate transistor.

60. (Original) The electronic fuse of Claim 58, wherein said first nonvolatile memory element comprises a first capacitor having a first plate in common with said first floating gate of

said first floating-gate transistor and said second nonvolatile memory element further comprises a second capacitor having a first plate in common with said second floating gate.

61. (Original) The electronic fuse of Claim 55, wherein said first and second nonvolatile memory elements comprise nonvolatile memory elements manufactured in a MOS fabrication process.

62. (Original) The electronic fuse of Claim 58, wherein at least one of said first and said second floating-gate transistors are MOS devices.

63. (Canceled)

64. (Original) The electronic fuse of Claim 58, wherein the amount of charge on at least one of said first and second floating gates may be changed using Fowler-Nordheim tunneling.

65. (Original) The electronic fuse of Claim 58, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot electron injection.

66. (Original) The electronic fuse of Claim 58, wherein the amount of charge on at least one of said first and second floating gates may be changed using direct tunneling.

67. (Original) The electronic fuse of Claim 58, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot-hole injection.

68. (Canceled)

69. (Original) The electronic fuse of Claim 59, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

70. (Original) The electronic fuse of Claim 69, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

71. (Original) The electronic fuse of Claim 55, further comprising a capacitive load coupled to an output of the latch.

72. (Original) The electronic fuse of claim 58, wherein the latch is predisposed to settle into one of said first and second states in response to voltages of said first and second floating gates.

73. (Original) The electronic fuse of claim 72, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

74. (Original) The electronic fuse of claim 72, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

75. (Original) The electronic fuse of claim 72, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

76. (Currently amended) An electronic fuse, comprising:

a latch having two cross-coupled inverters;

a first nonvolatile memory element coupled between a first power source or reset terminal of the fuse and a first of the two inverters of the latch; and

a second nonvolatile memory element coupled between the first power source or reset terminal of the fuse and a second of the two inverters of the latch,

wherein said first and second nonvolatile memory elements each comprises a pair of floating gate devices sharing a common floating gate, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

77. (Original) The electronic fuse of Claim 76, wherein the first and second nonvolatile memory elements are configured to be programmed to first and second memory values, respectively, said first and second memory values capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse.

78. (Original) The electronic fuse of Claim 77, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value.

79. (Original) The electronic fuse of Claim 78, wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value.

80. (Original) The electronic fuse of Claim 78, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

81. (Original) The electronic fuse of Claim 80, wherein said first nonvolatile memory element comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor said second nonvolatile memory element further comprises a second capacitor having a first plate in common with said second floating gate.

82. (Original) The electronic fuse of Claim 77, wherein said first and second nonvolatile memory elements comprise nonvolatile memory element manufactured in a MOS fabrication process.

83. (Original) The electronic fuse of Claim 79, wherein at least one of said first and second floating-gate transistors are MOS devices.

84. (Canceled)

85. (Original) The electronic fuse of Claim 79, wherein the amount of charge on at least one of said first and second floating gates may be changed using Fowler-Nordheim tunneling.

86. (Original) The electronic fuse of Claim 79, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot electron injection.

87. (Original) The electronic fuse of Claim 79, wherein the amount of charge on at least one of said first and second floating gates may be changed using direct tunneling.

88. (Original) The electronic fuse of Claim 79, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot-hole injection.

89. (Canceled)

90. (Original) The electronic fuse of Claim 80, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

91. (Original) The electronic fuse of Claim 90, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

92. (Original) The electronic fuse of Claim 76, further comprising a capacitive load coupled to an output of one of the inverters of the latch.

93. (Original) The electronic fuse of claim 79, wherein the latch is predisposed to settle into one of said first and second states in response to voltages of said first and second floating gates.

94. (Original) The electronic fuse of claim 93, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

95. (Original) The electronic fuse of claim 93, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

96. (Original) The electronic fuse of claim 93, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

97. (Currently amended) An electronic fuse, comprising:

a latch having two cross-coupled inverters;

a first nonvolatile memory element coupled in parallel with a transistor of a first of the two inverters of the latch; and

a second nonvolatile memory element coupled in parallel with a transistor of a second of the two inverters of the latch,

wherein said first and second nonvolatile memory elements each comprises a pair of floating gate devices sharing a common floating gate, said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is

associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.

98. (Previously presented) The electronic fuse of Claim 97, wherein the first and second nonvolatile memory elements are configured to be programmed to first and second memory values, respectively, said first and second memory values capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse.

99. (Original) The electronic fuse of Claim 98, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value.

100. (Original) The electronic fuse of Claim 99, wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value.

101. (Original) The electronic fuse of Claim 99, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

102. (Original) The electronic fuse of Claim 100, wherein said first nonvolatile memory element comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor said second nonvolatile memory element further comprises a second capacitor having a first plate in common with said second floating gate.

103. (Original) The electronic fuse of Claim 98, wherein said first and second nonvolatile memory elements comprise nonvolatile memory element manufactured in a MOS fabrication process.

104. (Original) The electronic fuse of Claim 100, wherein at least one of said first and second floating-gate transistors are MOS devices.

105. (Canceled)

106. (Original) The electronic fuse of Claim 100, wherein the amount of charge on at least one of said first and second floating gates may be changed using Fowler-Nordheim tunneling.

107. (Original) The electronic fuse of Claim 100, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot electron injection.

108. (Original) The electronic fuse of Claim 100, wherein the amount of charge on at least one of said first and second floating gates may be changed using direct tunneling.

109. (Original) The electronic fuse of Claim 100, wherein the amount of charge on at least one of said first and second floating gates may be changed using hot-hole injection.

110. (Canceled)

111. (Original) The electronic fuse of Claim 101, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

112. (Original) The electronic fuse of Claim 111, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

113. (Original) The electronic fuse of Claim 97, further comprising a capacitive load coupled to an output of one of the inverters of the latch.

114. (Original) The electronic fuse of claim 100, wherein the latch is predisposed to settle into one of said first and second states in response to voltages of said first and second floating gates.

115. (Original) The electronic fuse of claim 114, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

116. (Original) The electronic fuse of claim 114, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

117. (Original) The electronic fuse of claim 114, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

In the Drawings

The attached replacement and annotated sheet(s) of drawings include changes to FIGS. * as follows:

FIG. 12B has been amended to add the designations pFET and nFET.

FIG. 18 has been amended to add the designations 74', 76', 78' and 80'.

FIG. 19 has been amended to add the designations 153 and 155.

Attachment: Replacement sheet(s)
Annotated sheet(s) showing changes